

The diagram illustrates a PLL system. A **REFERENCE SIGNAL** is input to a **PHASE COMPARATOR** (23). The output of the phase comparator is a voltage V_t that passes through a **LOOP FILTER** (24) to the **VCO** (21). The VCO output is a **MODULATION SIGNAL** (31) and a voltage V_m . The V_m signal is fed back to the **PHASE COMPARATOR** (23). The V_m signal is also divided by a **DIVIDER** (22) to produce a signal for a **DIVIDING RATIO GENERATING PORTION** (27). This portion receives **CARRIER FREQUENCY DATA** and outputs a signal fc_1 to a **SELECTOR** (26). The **SELECTOR** (26) also receives **CALIBRATION DATA GENERATING PORTION** (25) and outputs a signal fc_2 to another **SELECTOR** (28). The **SELECTOR** (28) also receives **PHASE MODULATION DATA** and outputs a signal to a **CONTROL SIGNAL GENERATING PORTION** (30). This portion outputs a **MODULATION DEGREE CONTROL SIGNAL** to **MODULATION DEGREE CONTROLLING MEANS** (32). The **MODULATION DEGREE CONTROLLING MEANS** (32) also receives the **MODULATION SIGNAL** (31) and outputs a control signal to a **DEMODULATOR** (31).

2/9

FIG. 2

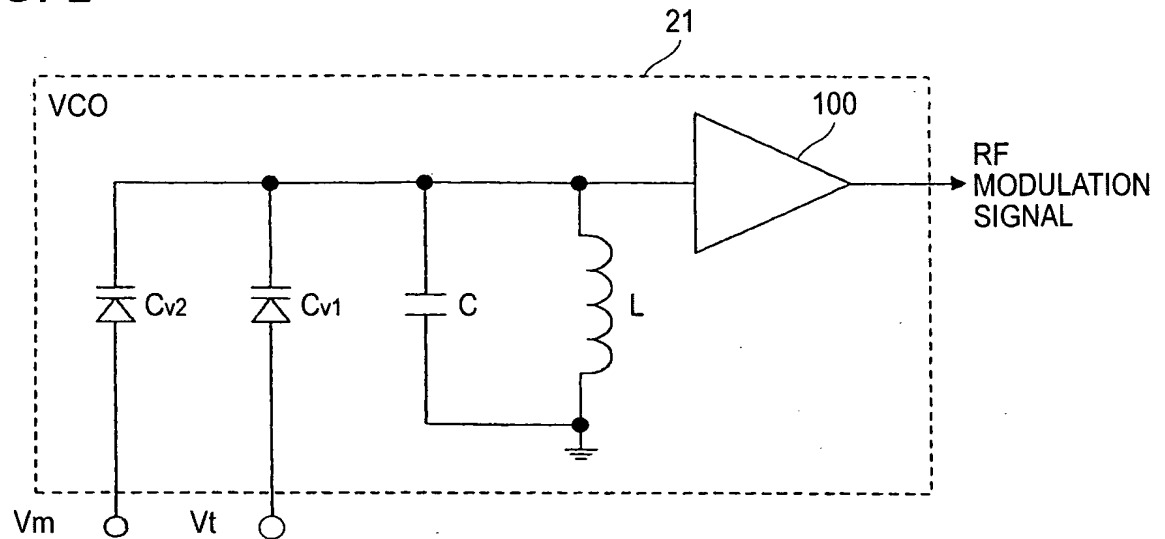


FIG. 3

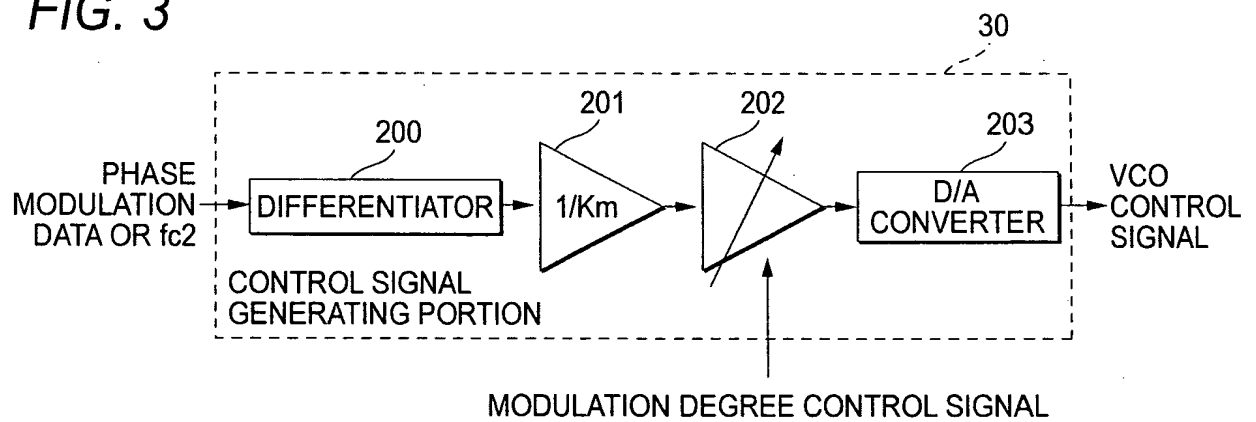
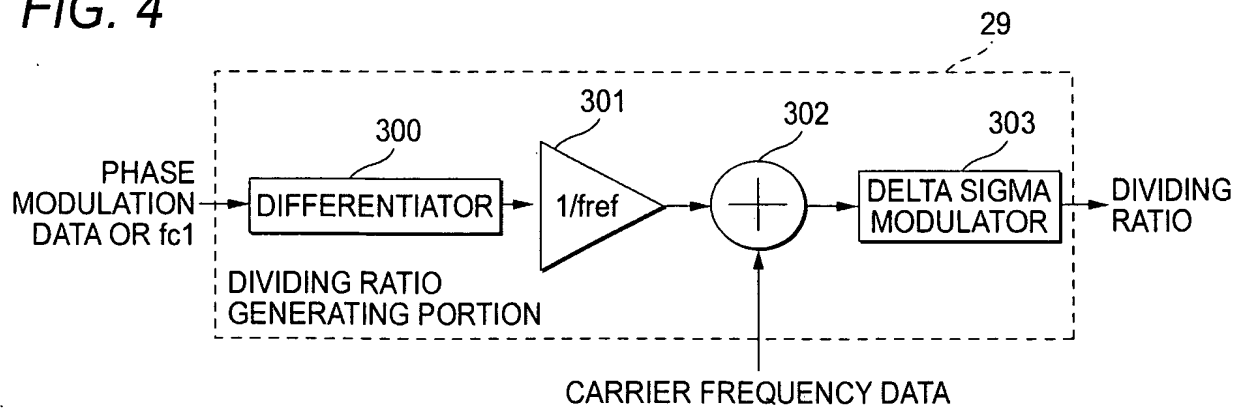


FIG. 4



3/9

FIG. 5

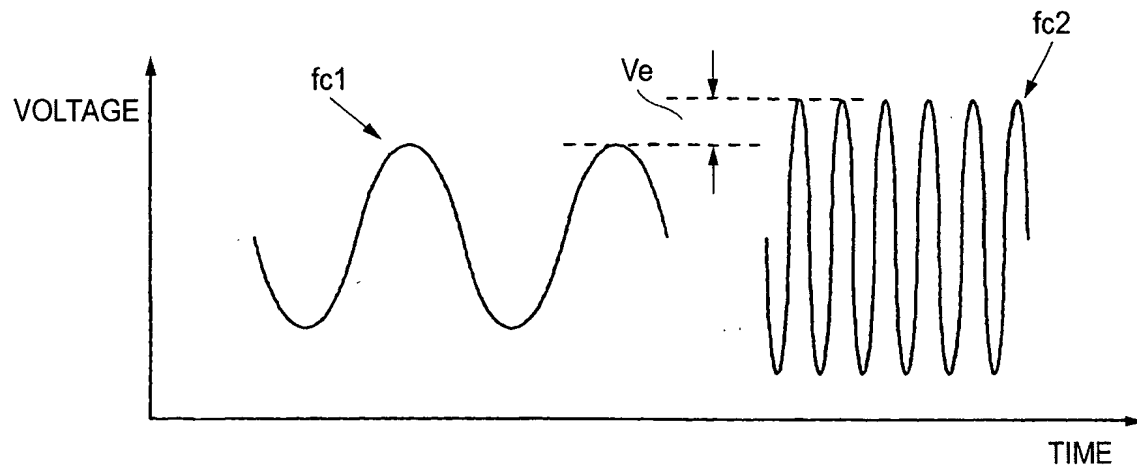
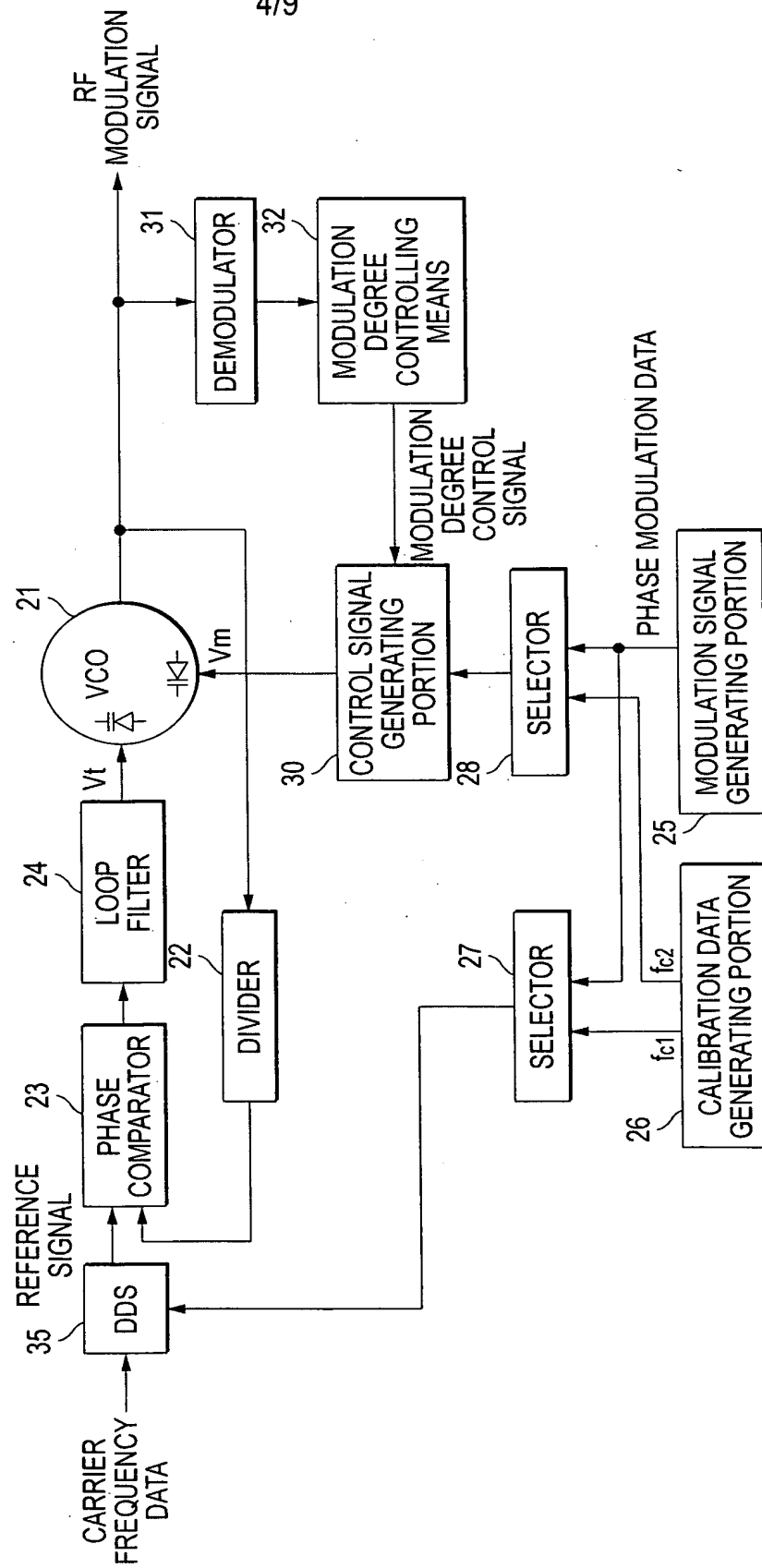
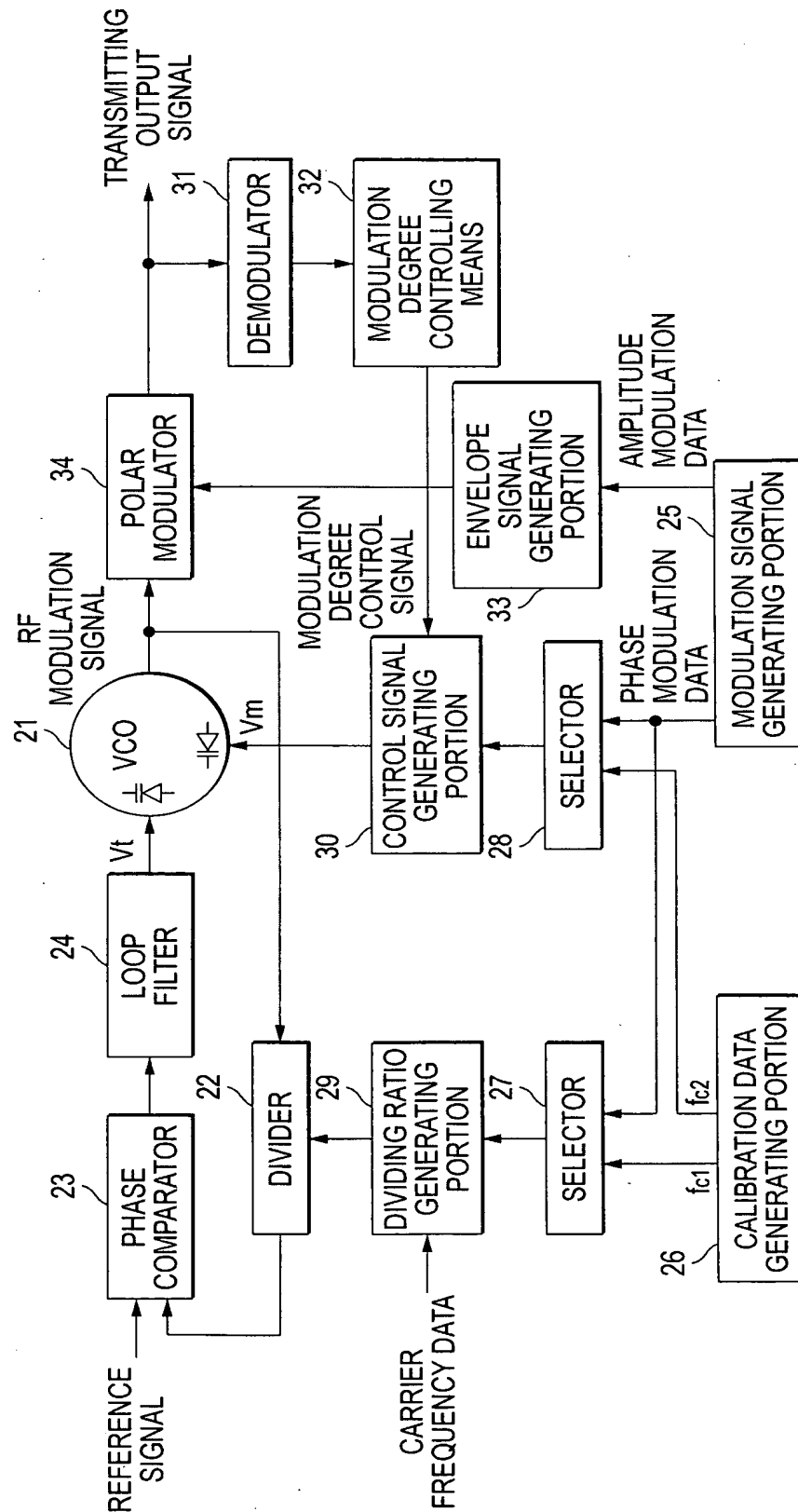


FIG. 6



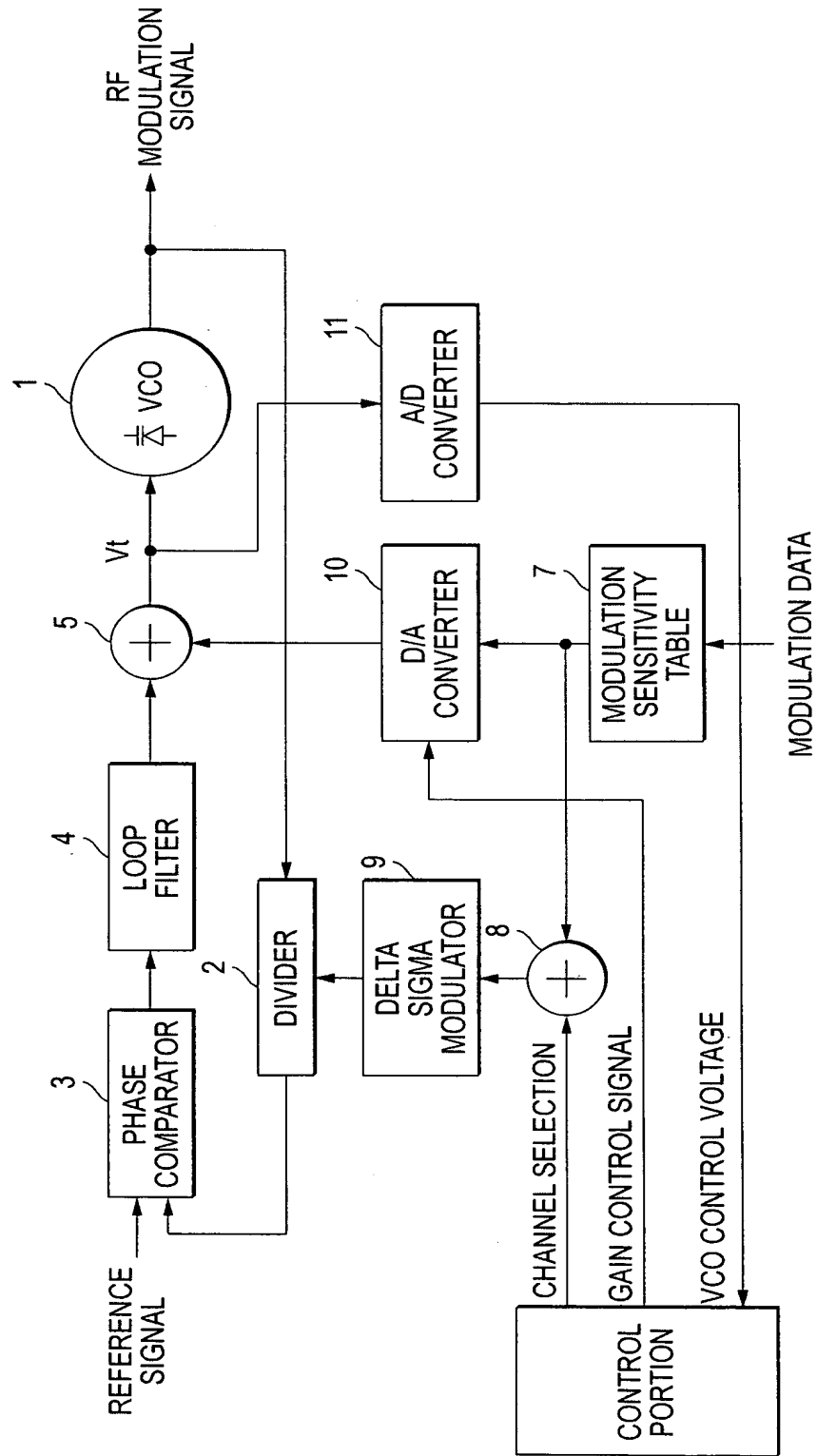
5/9

FIG. 7



6/9

FIG. 8



7/9

FIG. 9

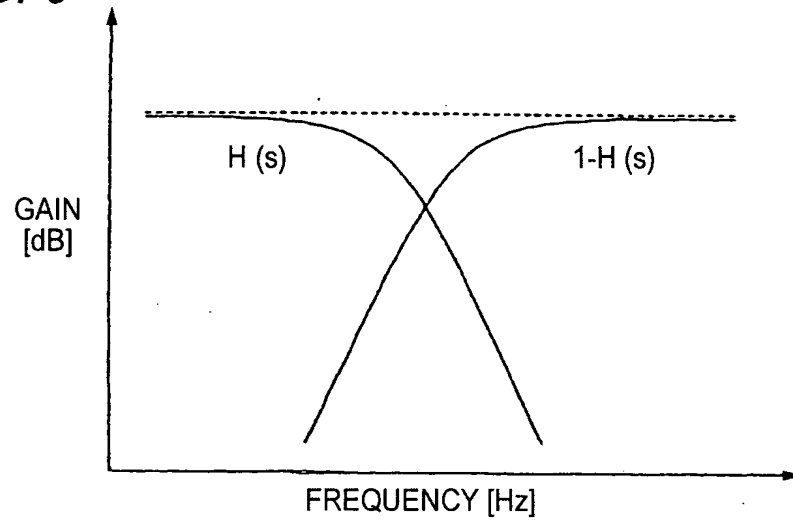
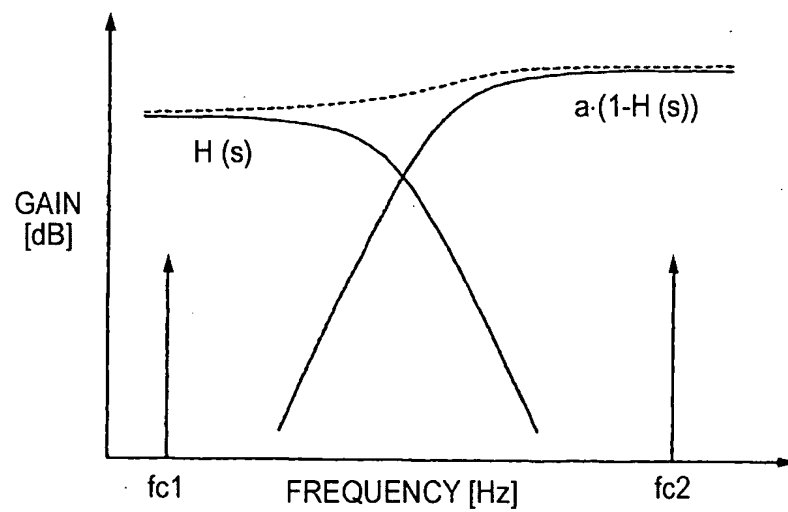


FIG. 10



8/9

FIG. 11

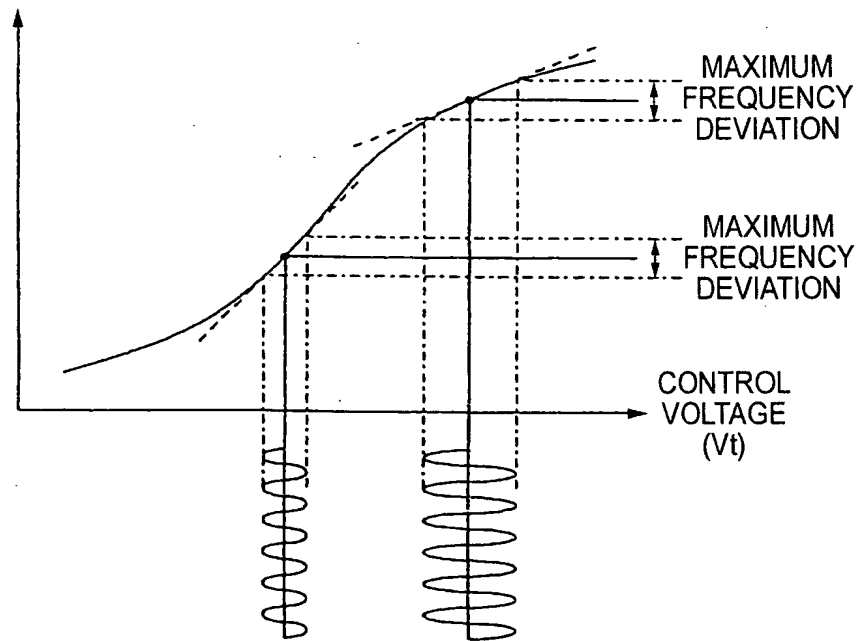
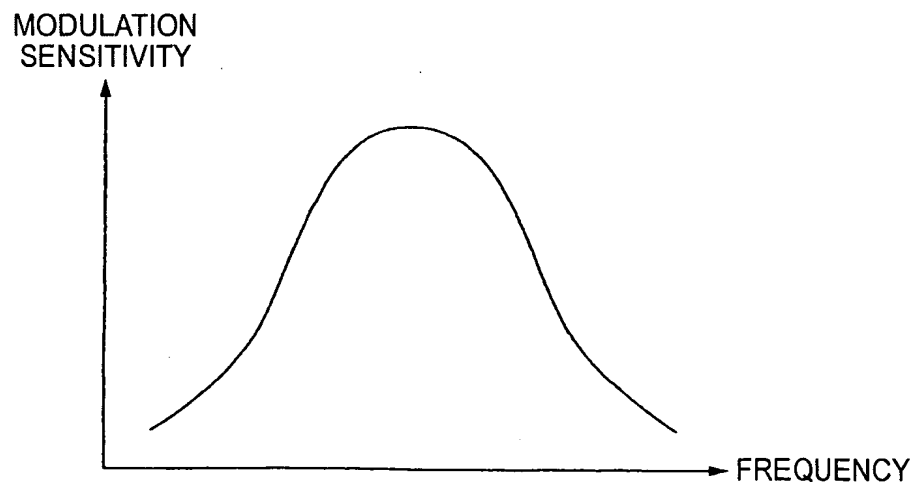


FIG. 12



9/9

FIG. 13

